R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

IN THE DRAWINGS

FIG. 1 has been amended to add the signal LOSSEL at the output of the element 110. Support for the amendment may be found on pages 6 and 7 of the specification as filed. No new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 5, 9-10, 15 and 19 under 35 U.S.C. §112, second paragraph, has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-20 under 35 U.S.C. §102 as being anticipated by Zhou has been obviated by appropriate amendment and should be withdrawn.

Zhou discloses a matched filter and signal reception apparatus (Title).

In contrast, claim 1 of the present invention provides an apparatus comprising a sample circuit and a selection circuit. The sample circuit may be configured to (i) detect a state of an input

signal and (ii) present a plurality of intermediate signals each representative of the state of the input signal during a plurality of clock cycles. The selection circuit may be configured to present a filtered signal in response to (i) a selected number of the intermediate signals having a lost state and (ii) a multi-bit selection signal representing a filtering value. The filtered signal indicates the input signal has been lost when the selected number lost states is greater than the filtering value. Claims 11 and 20 have similar limitations. Zhou does not disclose or suggest such an apparatus or method.

In particular, the so-called second circuit (or selection circuit) of Zhou does not appear to respond to a multi-bit selection signal representing a filtering value, as presently claimed. The so-called second circuit of Zhou (the circuit SEL1, the circuit M1, and the circuit XOR1) does not appear to receive such a multi-bit selection signal. At best, the signal M1 presents a signal the most similar to the claimed multi-bit selection signal. However, the signal M1 (which is not described in detail in FIG. 13, but is described in more detail in connection with FIG. 2 of Zhou) describes the signal M1 as a "spreading code" (see column 3, lines 52-67 of Zhou). In particular, Zhou describes that "when the bit of the spreading code is "1" the digital bits corresponding to the analog input are inverted . . . this is equivalent to **a multiplication by the spreading code**". Clearly,

the presently claimed invention is not concerned with multiplying, as in Zhou. In contrast, the presently claimed multi-bit selection signal is used to control the filtering of the selection circuit. In particular, the filtered signal indicates that the input signal has been lost when the selected number of lost states is greater than the filtering value. Zhou is silent regarding such a filtering value or such a filtered signal. Zhou does not disclose or suggest each and every element of the claimed invention and the rejection should be withdrawn.

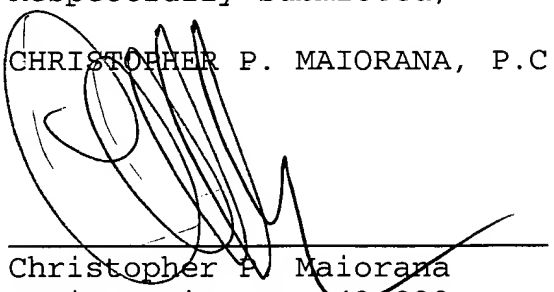
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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Docket No.: 01-349 / 1496.00141

REPLACEMENT SHEET

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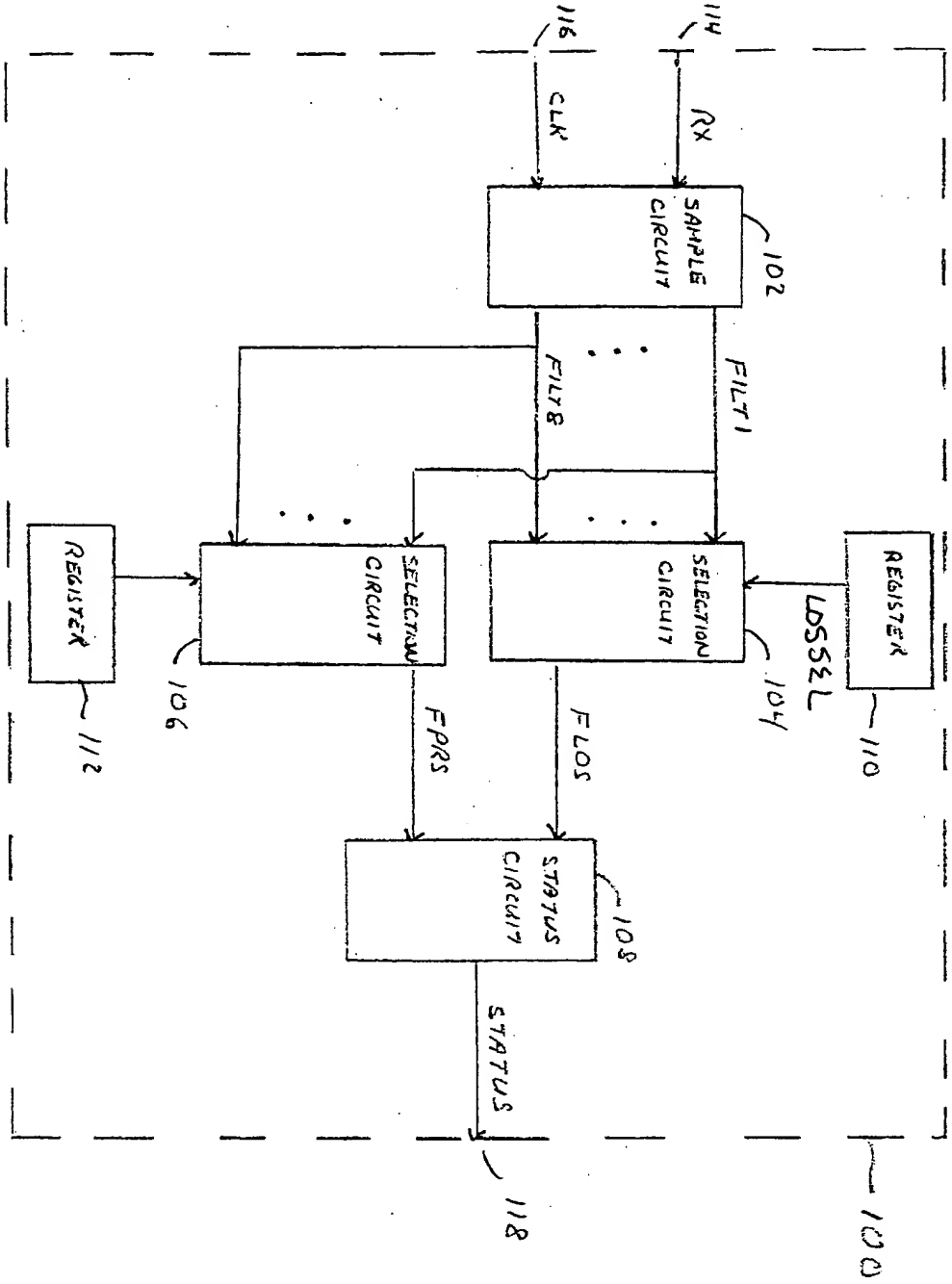

FIG. 1